Binary logic using spatially patterned deaths in chemical oscillators

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Synchronisation amongst chemical reaction-diffusion systems or 'chemical-oscillators' has been studied in detail both experimentally and theoretically [1, 2]. The temporal evolution of certain reaction solutions in microfluidic assemblies [3] gives interesting spatial patterns (e.g. Belousov-Zhabotinsky reaction). We use the FitzHugh-Nagumo (FHN) model to mimic these spatiotemporal patterns and explore the possibility of constructing 'logic gates' [4] using such oscillators.

The FHN model consists of two variables viz. fast activation variable, u and slow inactivation variable v, also known as the excitatory and inhibitory variables respectively. The excitatory variable has a cubic nonlinearity, and the inhibitory variable has a linear behaviour. The model is described as follows:

$$\dot{u} = f(u, v) = u(1-u)(u-\alpha) - v \tag{1a}$$

$$\dot{v} = g(u, v) = \epsilon(ku - v - b) \tag{1b}$$

where the parameters α and k describe the kinetics, ϵ characterises the recovery rate, and b is a measure of the asymmetry of an entity in the system.

We considered a system of N relaxation oscillators, interacting in some particular topological configuration. The FHN equations dictate the dynamics of each oscillator. The values of the parameters used are: $\alpha = 0.139$, $k = 0.6$ and $\epsilon = 0.001$. The neighbouring oscillators are coupled diffusively via the inactivation variable v. Dynamics of the resulting system can be given as follows.

$$\dot{u_i} = f(u_i, v_i) \tag{2a}$$

$$\dot{v_i} = g(u_i, v_i) + D_v(v_{i-1} + v_{i+1} - 2v_i) \tag{2b}$$

$$\dot{v_0} = D_v(v_1 - v_0) \tag{2c}$$

$$\dot{v}_{N+1} = D_v(v_N - v_{N+1}) \tag{2d}$$

Here $i = 1, 2, ..., N$ and D_v represents the strength of the coupling between neighbouring relaxation oscillators through the inhibitory variables. For various regions in the $b - D_v$ domain, interesting spatiotemporal patterns are obtained. Our work was concentrated with the spatially patterned oscillator deaths (SPOD). The SPOD state is most suited for developing logic gates because a) information can easily be encoded into the SPOD states in the form of binaries. The high modes can be assigned the value 1 and the low ones 0. b) The SPOD state remains steady with the evolution of time unless a change is triggered externally. This is desirable for computation because the information stored should not alter unless an external stimulus is provided.

The SPOD state can be obtained for only certain regions in the $b - D_v$ space; we considered values of b and D_v to be in the vicinity 0.16 and 0.002, however, these choices are not unique. We considered a system of 20 oscillators, in which the value attained by the 10^{th} and the 11^{th} oscillators were taken as inputs. A perturbation of a finite amplitude was applied for a certain time duration to different configurations of oscillators. This induced changes in the values attained by the oscillators. The value attained by the 11^{th} oscillator was considered the output.

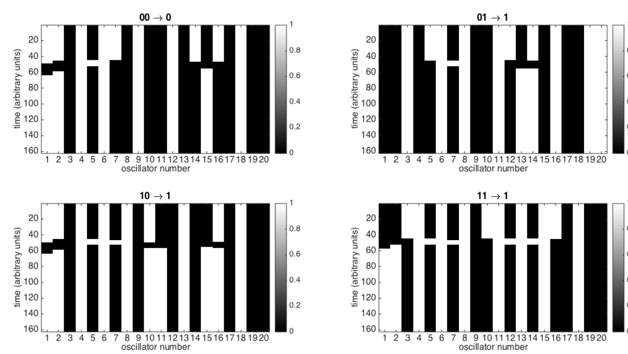

Figure 1: The OR gate constructed using SPOD logic

We successfully constructed a parity checker, an OR gate, a NOT gate and a NOR gate. The presence of the NOR gate ensures that universal computation is possible. We are still looking for the NAND gate and trying to establish if staggering of gates is possible. This would be a huge leap towards practical implementations of such gates.

References

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